

Amendments to the Claims:

1. (currently amended) A method for transmitting data in a multi-chip system, the multi-chip system comprising at least a host chip engaged in controlling operations of the multi-chip system, and at least a slave chip engaged in executing servo control or signal detection, the method comprising the following steps:
- 5 (a) the slave chip informing the host chip of data needed to be transmitted;
- (b) when being informed by the slave chip, the host chip informing the slave chip to start to transmit the data; and
- 10 (c) when being informed by the host chip, the slave chip starting to transmit the data to the host chip.
2. (original) The method of claim 1 wherein in step (b) the host chip
- 15 further delivers a clock signal to the slave chip.
3. (original) The method of claim 1 wherein in step (a) the slave chip actively alters a voltage on a request pin pair, electrically connected between the host chip and the slave chip, to inform the host
- 20 chip of the data needed to be transmitted.
4. (original) The method of claim 1 wherein in step (a) the slave chip detects states of a plurality of signals, when any changes of the states of the plurality of the signals are detected, the slave chip actively
- 25 alters a voltage on a request pin pair to inform the host chip of the data needed to be transmitted, wherein the request pin pair is electrically connected between the host chip and the slave chip.
5. (original) The method of claim 1 wherein in step (b) the host chip
- 30 detects a voltage on a request pin pair, when the host chip detects that the voltage on the request pin pair has changed, the host chip delivers a clock signal to the slave chip via a clock pin pair, wherein the request

pin pair and the clock pin pair are both electrically connected between the host chip and the slave chip.

6. (original) The method of claim 1 wherein in step (b) the host chip
5 alters a voltage on a latch pin pair for informing the slave chip to start transmitting the data, wherein the latch pin pair is electrically connected between the host chip and the slave chip.

7. (original) The method of claim 1 wherein in step (c) the slave
10 chip transmits the data to the host chip via a data pin pair on a basis of a clock signal of a clock pin pair, wherein the data pin pair and the clock pin pair are both electrically connected between the host chip and the slave chip.

8. (original) The method of claim 1 wherein in step (c) the slave
15 chip transmits states of a plurality of signals to the host chip via a data pin pair on a basis of a clock signal of a clock pin pair, wherein the data pin pair and the clock pin pair are both electrically connected between the host chip and the slave chip.

9. (original) The method of claim 1 wherein the method further
20 comprises the following step:

(d) the host chip receiving data from the slave chip and decoding the
data.

10. (previously presented) The method of claim 1 wherein the slave chip
25 is an analog chip and the host chip is a digital chip.

11. (previously presented) The method of claim 1 wherein the
30 multi-chip system is an optical disk drive.

12. (previously presented) The method of claim 11 wherein the slave

chip is a servo control chip and the host chip is for controlling operations of the optical disk drive.

13. (previously presented) The method of claim 11, wherein in step (b),
5 when being informed by the slave chip, the host chip further for delivering a clock signal to the slave chip, and when not being informed by the slave chip, the host chip not delivering the clock signal to the slave chip.
- 10 14. (previously presented) The method of claim 13 wherein in step (b) the host chip further delivering the clock signal to the slave chip having a predetermined number of clock cycles.
- 15 15. (previously presented) The method of claim 14 wherein in step (c) when being informed by the host chip, the slave chip transmitting a fixed number of servo signals to the host chip; wherein the fixed number is equal to the predetermined number and one servo signal is transmitted by the slave chip to the host chip during each clock cycle.
- 20 16. (previously presented) The method of claim 15 wherein at least one of the servo signals is a tracking servo signal.
17. (previously presented) The method of claim 15 wherein at least one of the servo signals is a focusing servo signal.
- 25 18. (previously presented) The method of claim 15 wherein at least one of the servo signals is a tray open signal.
19. (previously presented) The method of claim 15 wherein at least one of the servo signals is a tray close signal.
- 30 20. (previously presented) The method of claim 15 wherein at least

one of the servo signals is a disk blank signal.

21. (previously presented) The method of claim 15 wherein at least one of the servo signals is a disk defect signal.

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22. (new) A multi-chip system comprising:

a host chip for controlling operations of the multi-chip system and having a request pin, a data pin, a latch pin, and a clock pin; and

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a slave chip for executing servo control or signal detection and having a request pin, a data pin, a latch pin, and a clock pin;

wherein the pins of the slave chip are coupled to the same named pin of the host chip to thereby form a request pin pair, a data pin pair, a latch pin pair, and a clock pin pair between the host chip and the slave chip.

23. (new) The multi-chip system of claim 22, wherein when the slave chip has data needing to be transmitted to the host chip, the slave chip is for asserting a voltage on the request pin pair to thereby inform the host chip of the data needing to be transmitted.

24. (new) The multi-chip system of claim 23, wherein when detecting the asserted voltage on the request pin pair, the host chip is for starting to deliver a clock signal via the clock pin pair to the slave chip and for asserting a voltage on the latch pin pair to inform the slave chip to prepare for transmitting the data.

25. (new) The multi-chip system of claim 24, wherein the host chip is further for de-asserting the voltage on the latch pin pair a period of time after asserting the voltage on the latch pin pair to thereby inform the slave chip to start transmitting the data.

26. (new) The multi-chip system of claim 25, wherein the slave chip is further for transmitting the data sequentially to the host chip via the data pin pair on the basis of the clock signal upon the de-assertion of the voltage on the latch pin pair.

27. (new) The multi-chip system of claim 26, wherein the host chip is further for decoding the data received via the data pin pair from the slave chip on the basis of the clock signal.

28. (new) The multi-chip system of claim 27, wherein when the data has been fully transmitted from the slave chip to the host chip, the slave chip and the host chip are for holding the request pin pair, the data pin pair, the latch pin pair, and the clock pin pair at initial values while waiting for a next data transmission.